

The diagram illustrates a lithography system (1100). A light source (1104) emits a beam of light (dashed line) that is reflected by a mirror (1103) and then by another mirror (1105). The light then passes through a lens (1106) and is focused onto a wafer (1107) mounted on a stage (1109). The wafer (1107) is positioned above a substrate (1101). The stage (1109) is supported by a vertical column (1111). The entire system is labeled 1100.

FIG. 1 PRIOR ART

FIG.2A
PRIOR ART

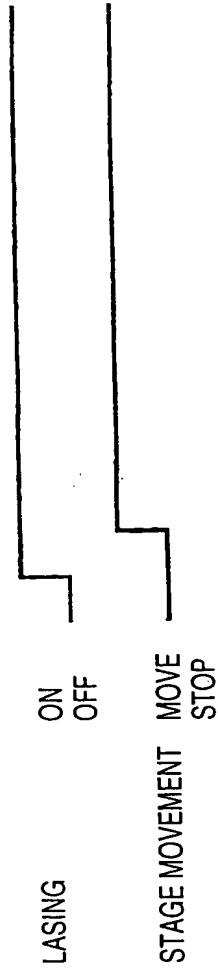


FIG.2B
PRIOR ART

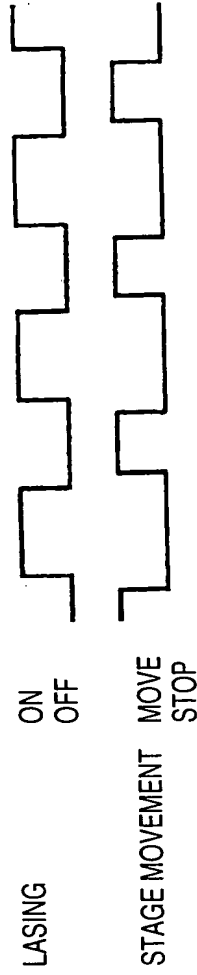


FIG.2C
PRIOR ART

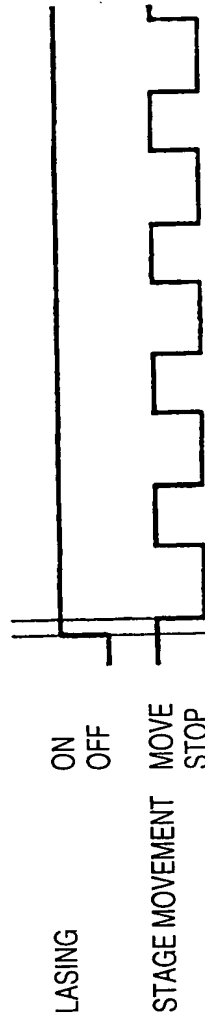
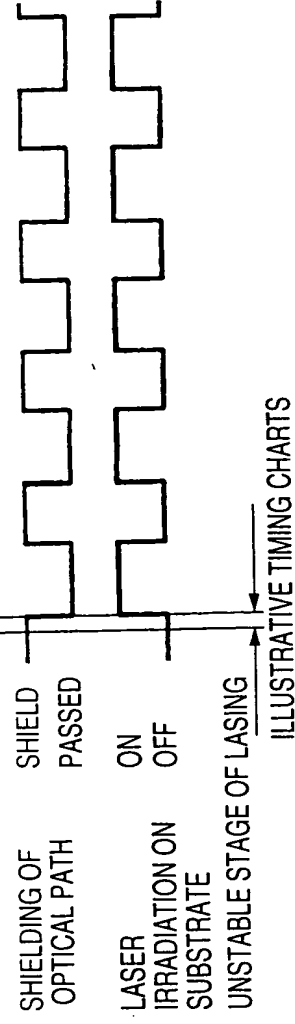


FIG.2D
PRIOR ART



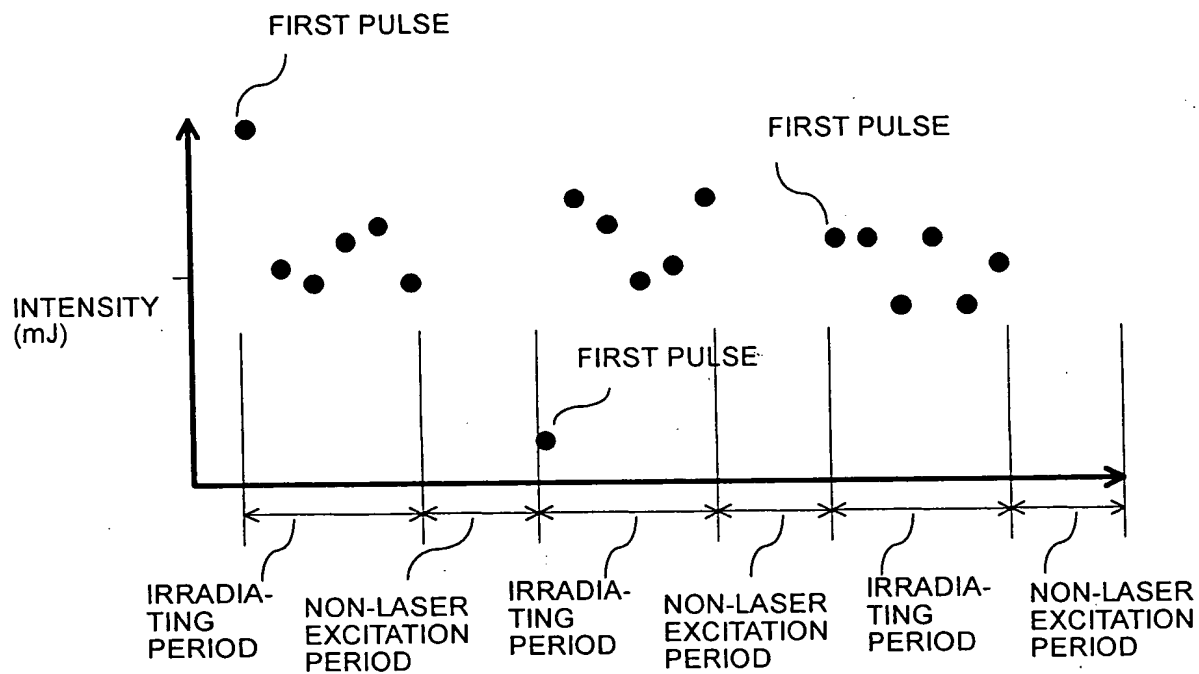


FIG. 3

000000 13531300

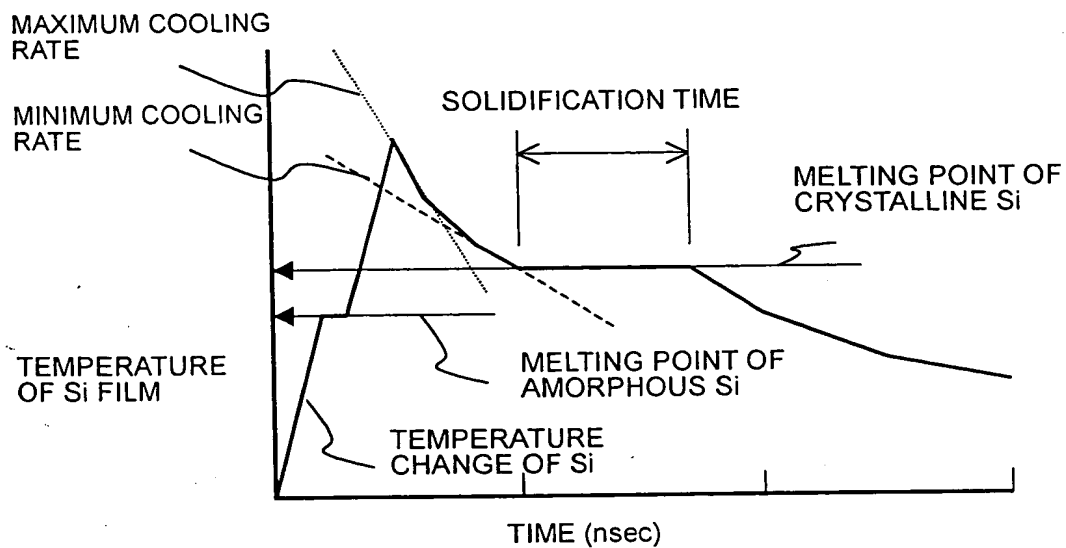
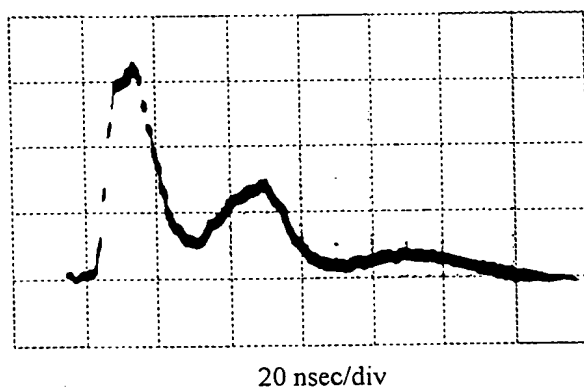
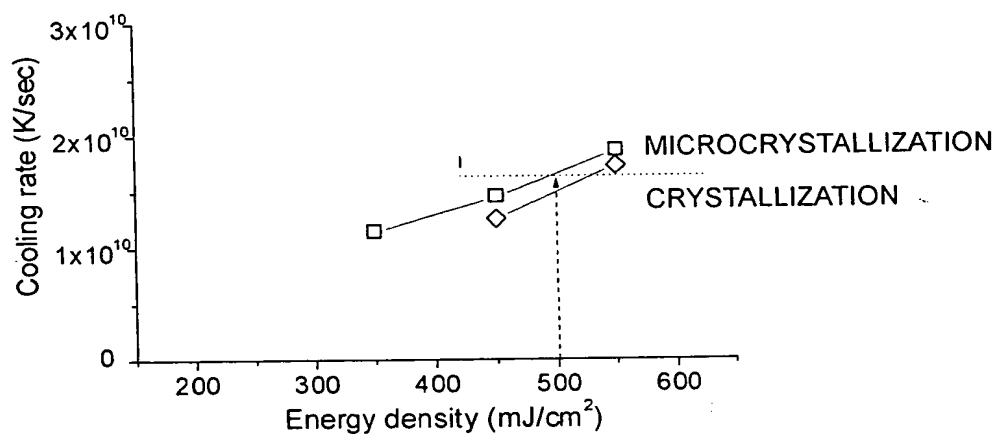


FIG. 4



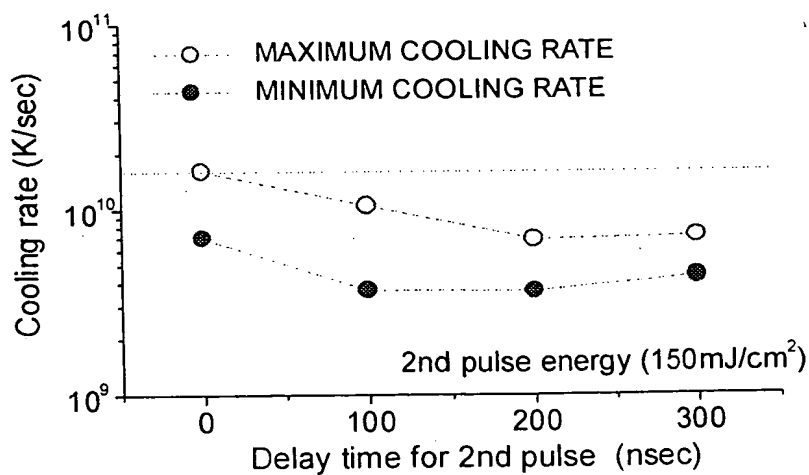
ILLUSTRATIVE LASER PULSE SHAPE

FIG. 5



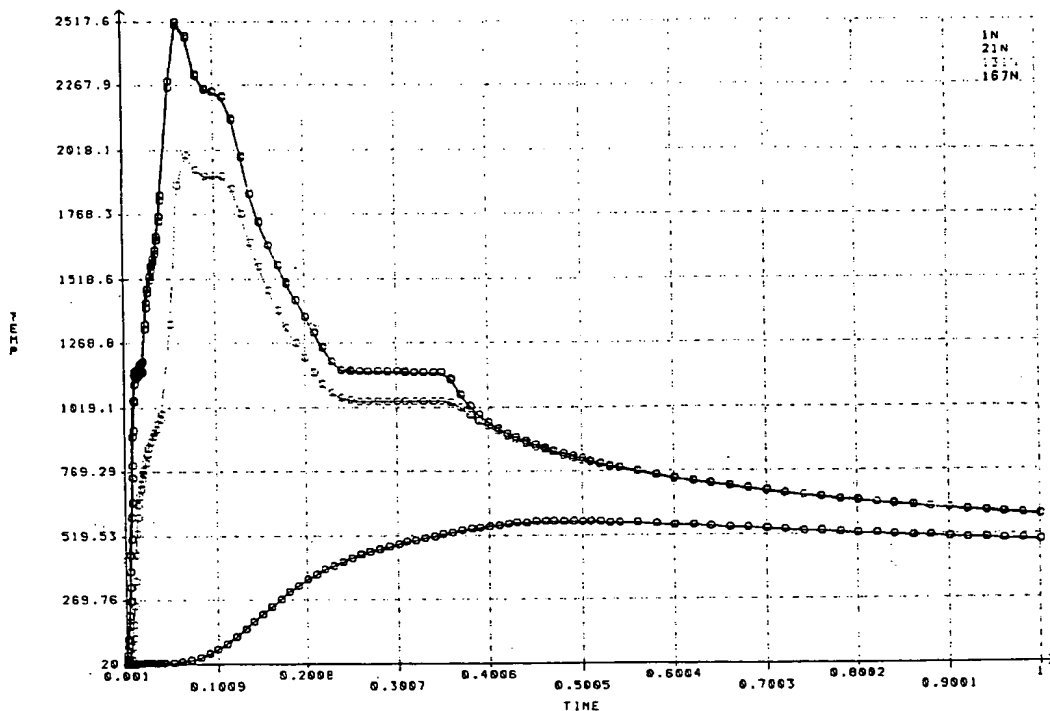
RELATIONSHIP BETWEEN IRRADIATION INTENSITY AND COOLING RATE, AND COOLING RATE AT WHICH THE MATERIAL BECOMES AMORPHOUS

FIG. 6



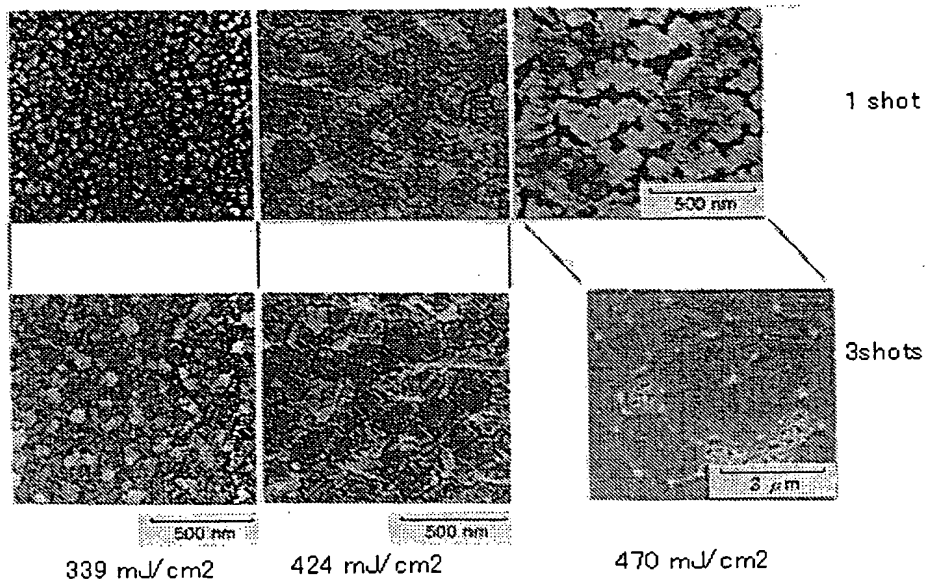
RELATIONSHIP BETWEEN MAXIMUM COOLING RATE AFTER APPLICATION OF SECOND PULSE AND THE COOLING RATE IN THE VICINITY OF SOLIDIFICATION POINT

FIG. 9



TEMPERATURE OF SILICON THIN FILM 75nm THICK ON A SiO_2 SUBSTRATE IRRADIATED AT AN INTENSITY OF $450\text{mJ}/\text{cm}^2$ BY XeCL LASER (WAVELENGTH: 308nm)

FIG. 7



ELECTRON MICROSCOPIC PHOTOGRAPHS OF LASER-INDUCED CRYSTALLIZED FILMS AFTER ZERO-ETCHING RELATIVE TO IRRADIATION INTENSITY AND NUMBER OF IRRADIATION TIME

FIG. 8

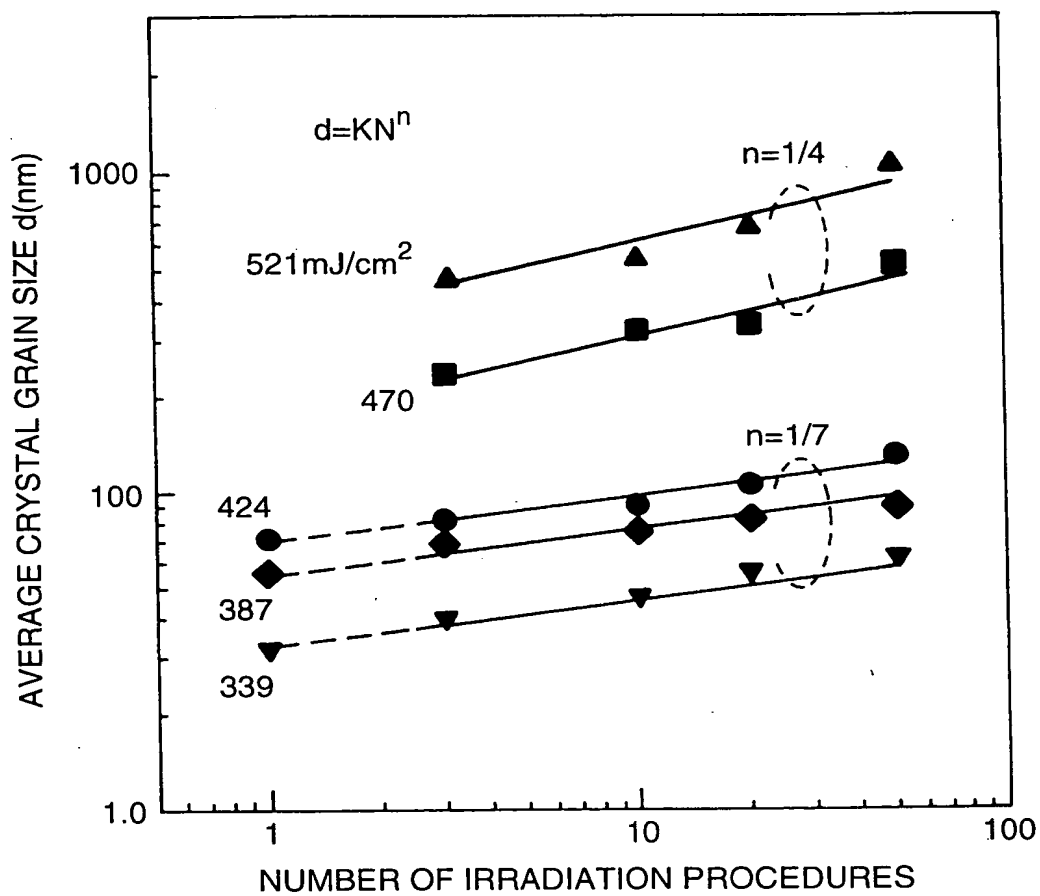


FIG.10

0064564-020700

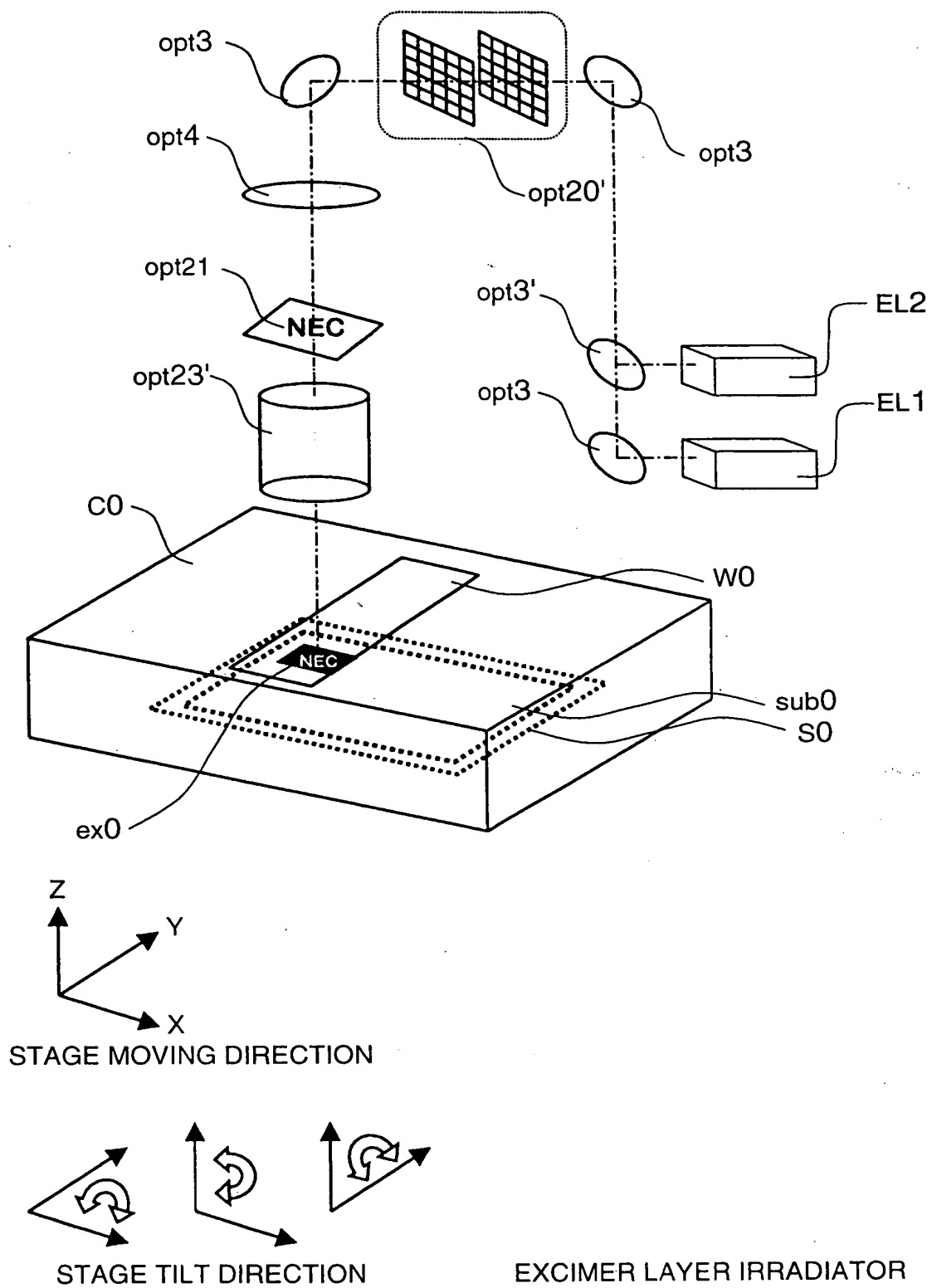


FIG.11

FIG.13A
MASK
PATTERN

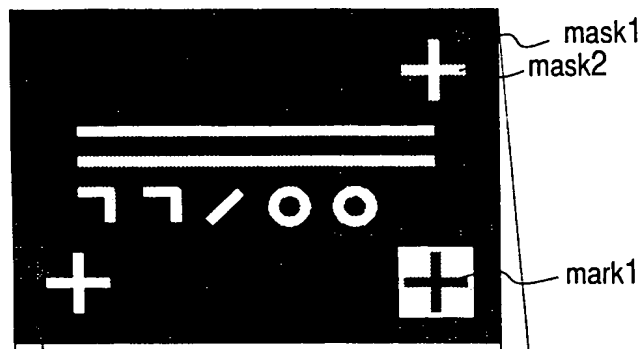


FIG.13B
EXPOSURE
PATTERN

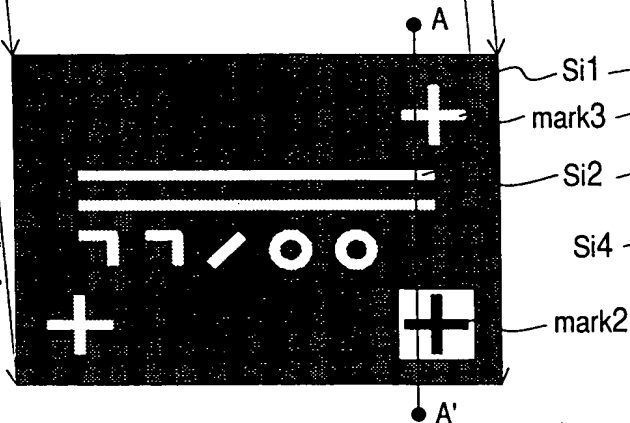
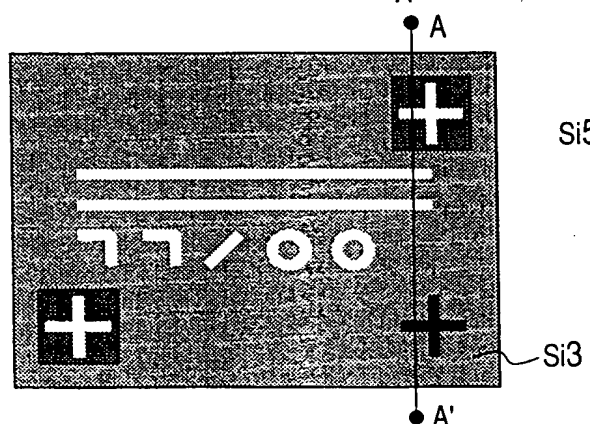


FIG.13D
ETCHING
PATTERN



A-A' CROSS SECTION

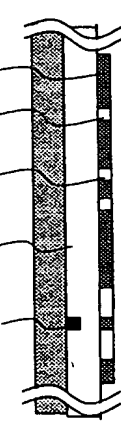


FIG.13C

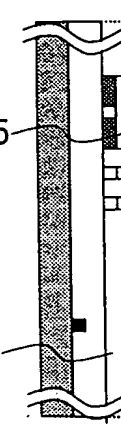


FIG.13E

PATTERN TRANSFER AND ALIGNMENT IN
EXCIMER LASER ANNEALING

ILLUSTRATIVE CONTROL PROCEDURE (1)

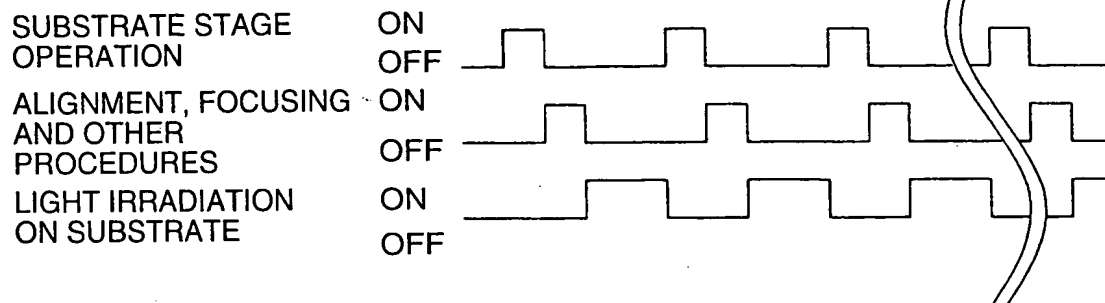


FIG.14A

ILLUSTRATIVE CONTROL PROCEDURE (2)

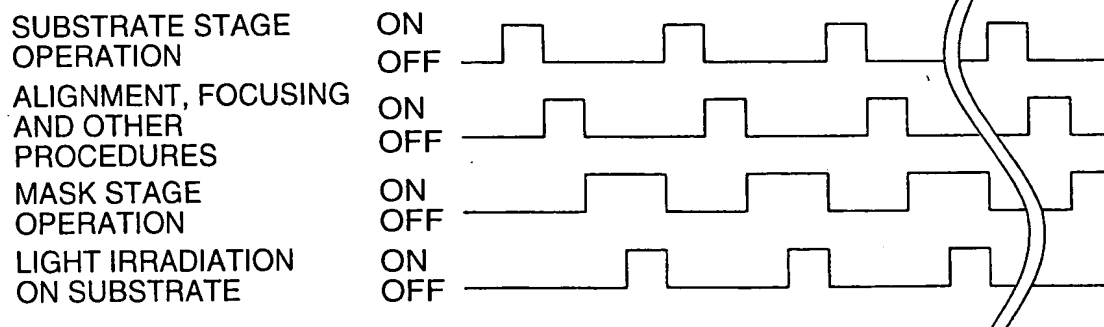
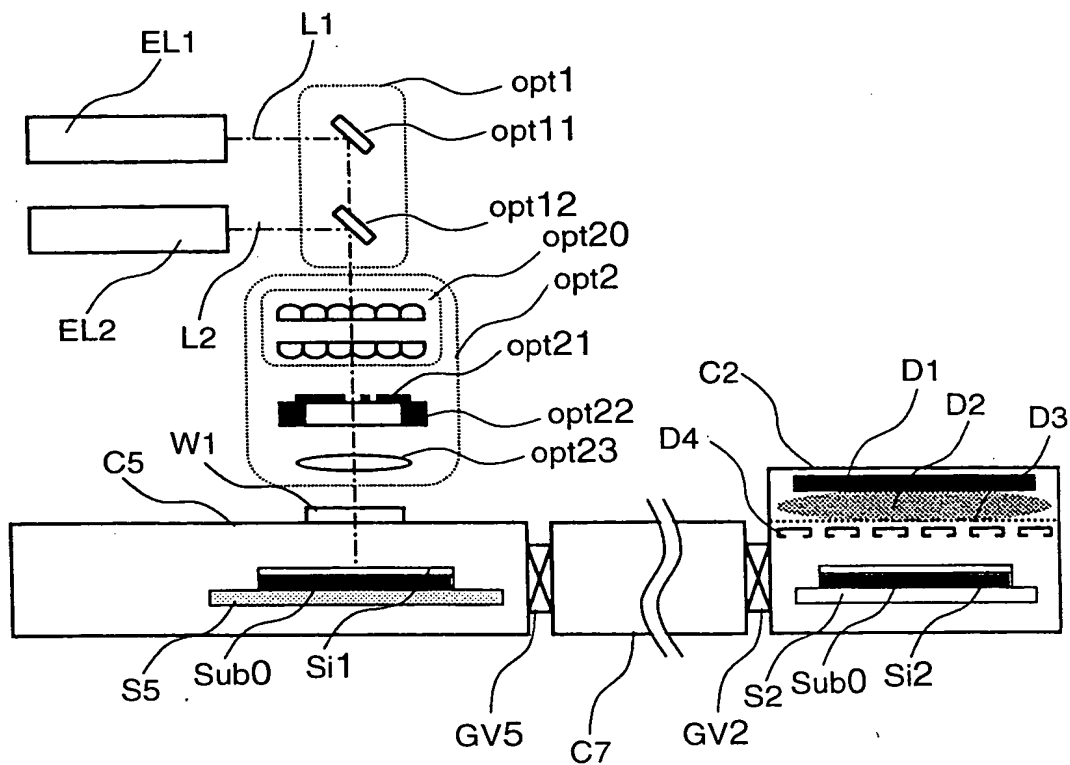


FIG.14B



PLASMA-ENHANCED CVD CHAMBER-SUBSTRATE TRANSFER
CHAMBER-LASER IRRADIATING CHAMBER

FIG.15

FIG. 16

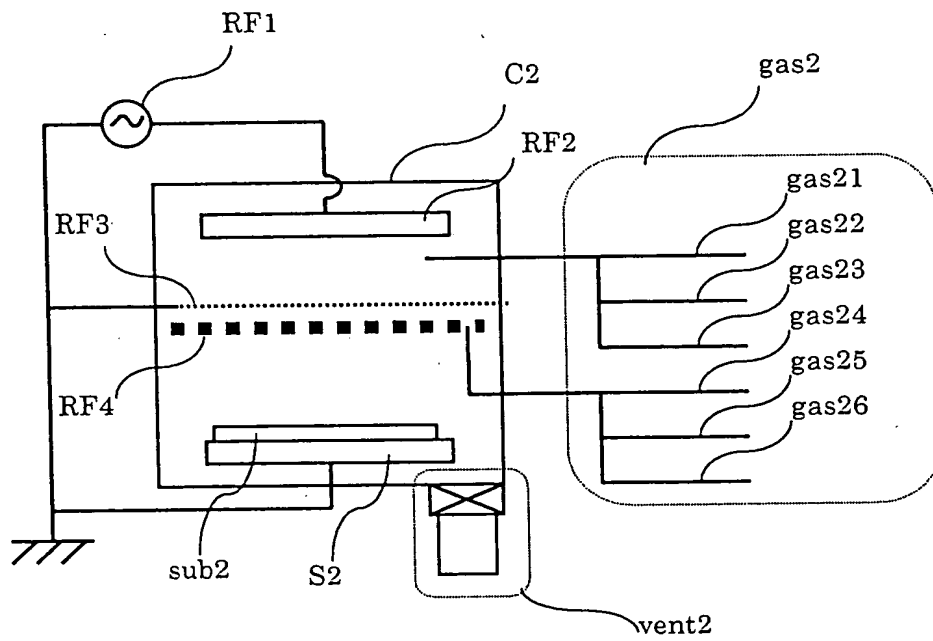


FIG. 17

FIG. 18G2

FIG. 19G2

FIG. 20F2

FIG.22A

FIRST LASING TRIGGER

FIG.22B

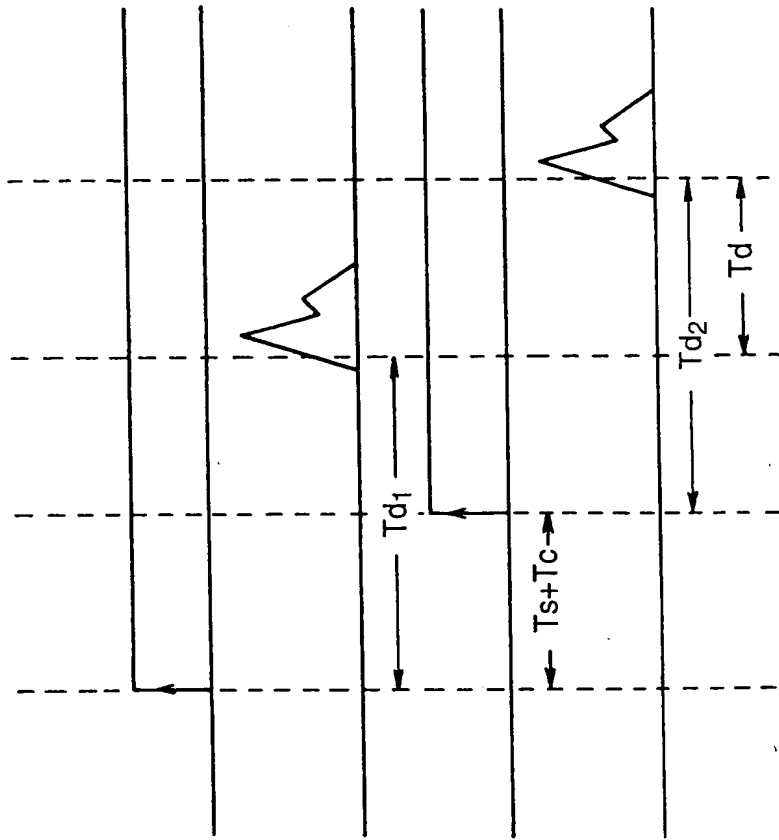
FIRST LASING PULSE

FIG.22C

TRIGGER DELAY CIRCUIT
OUTPUT / SECOND
LASING TRIGGER

FIG.22D

SECOND LASING PULSE



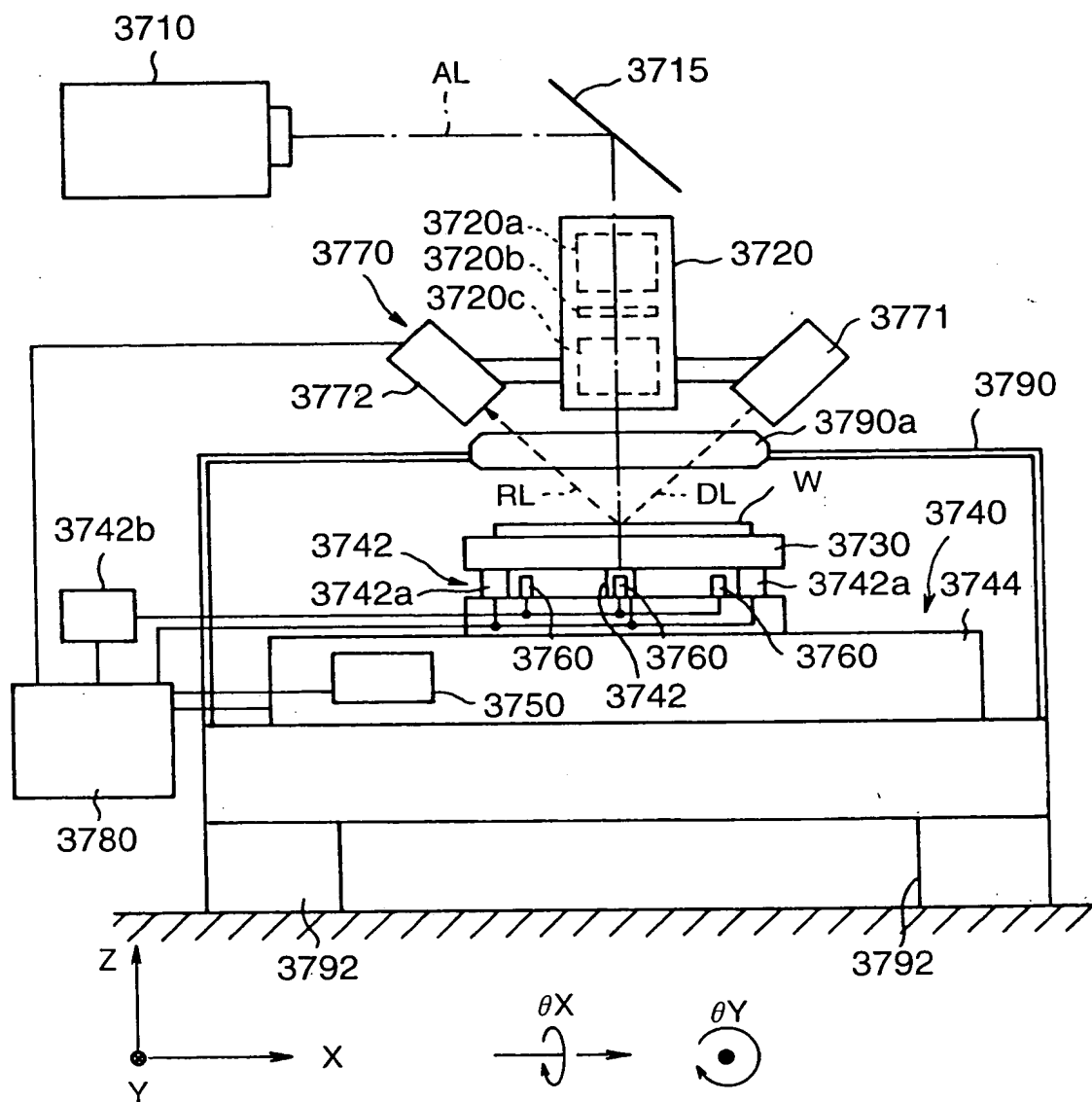


FIG.23

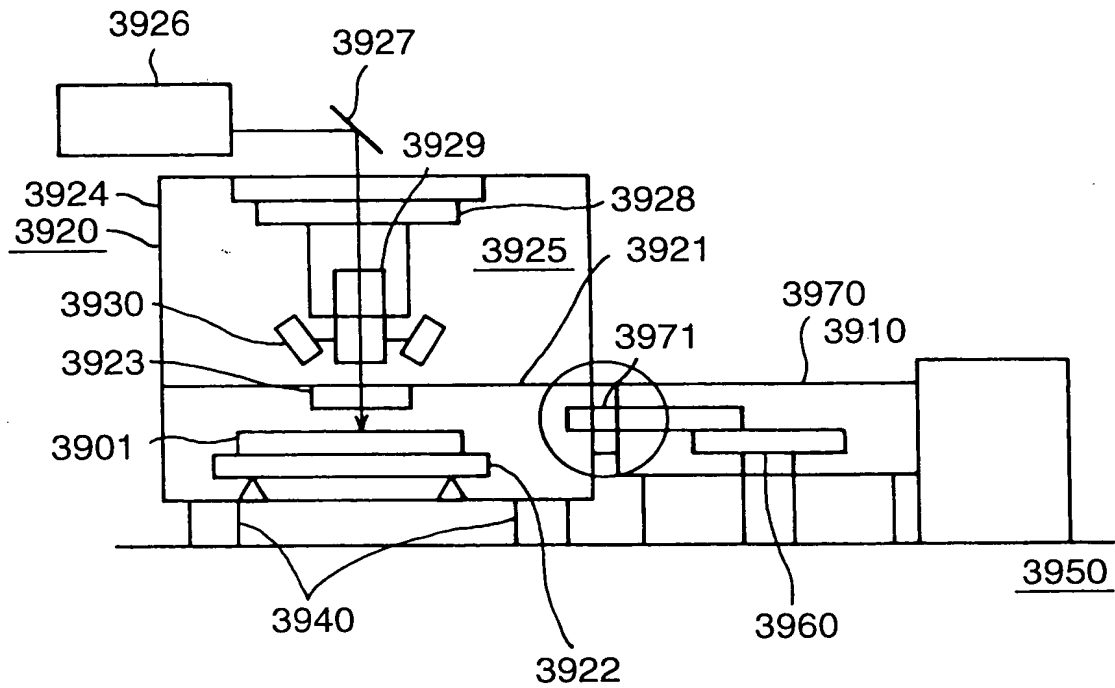


FIG.24

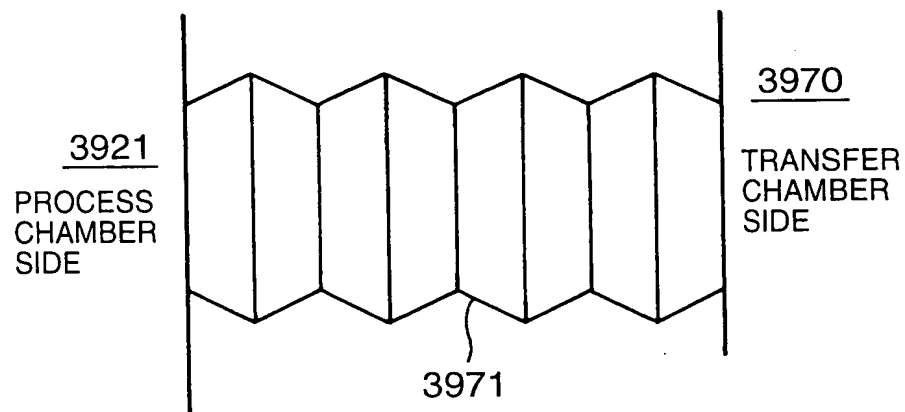
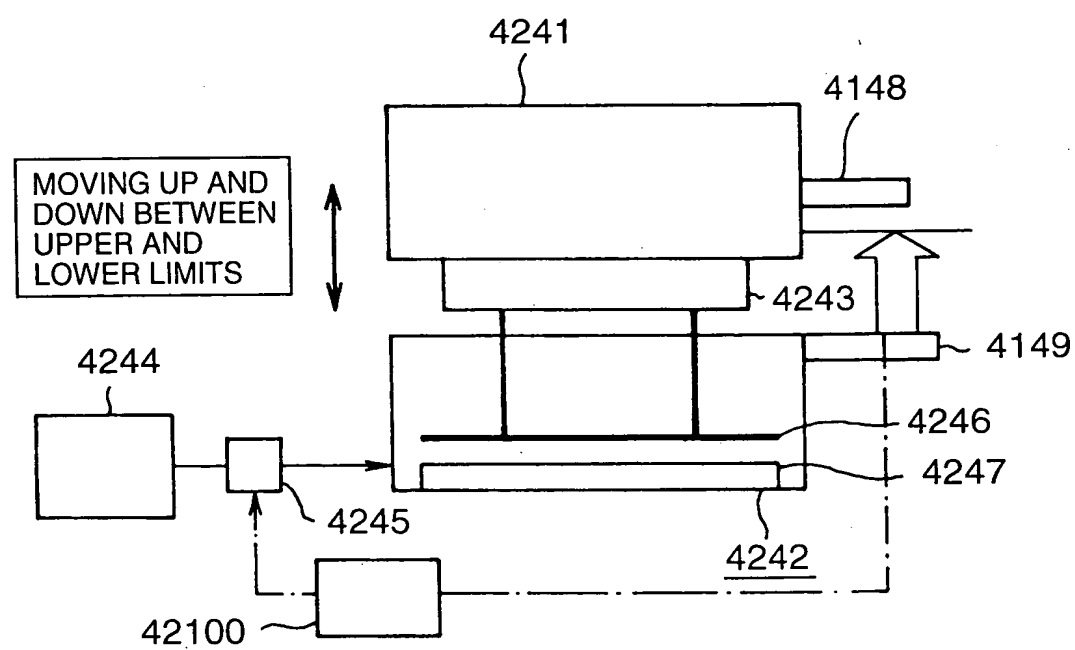
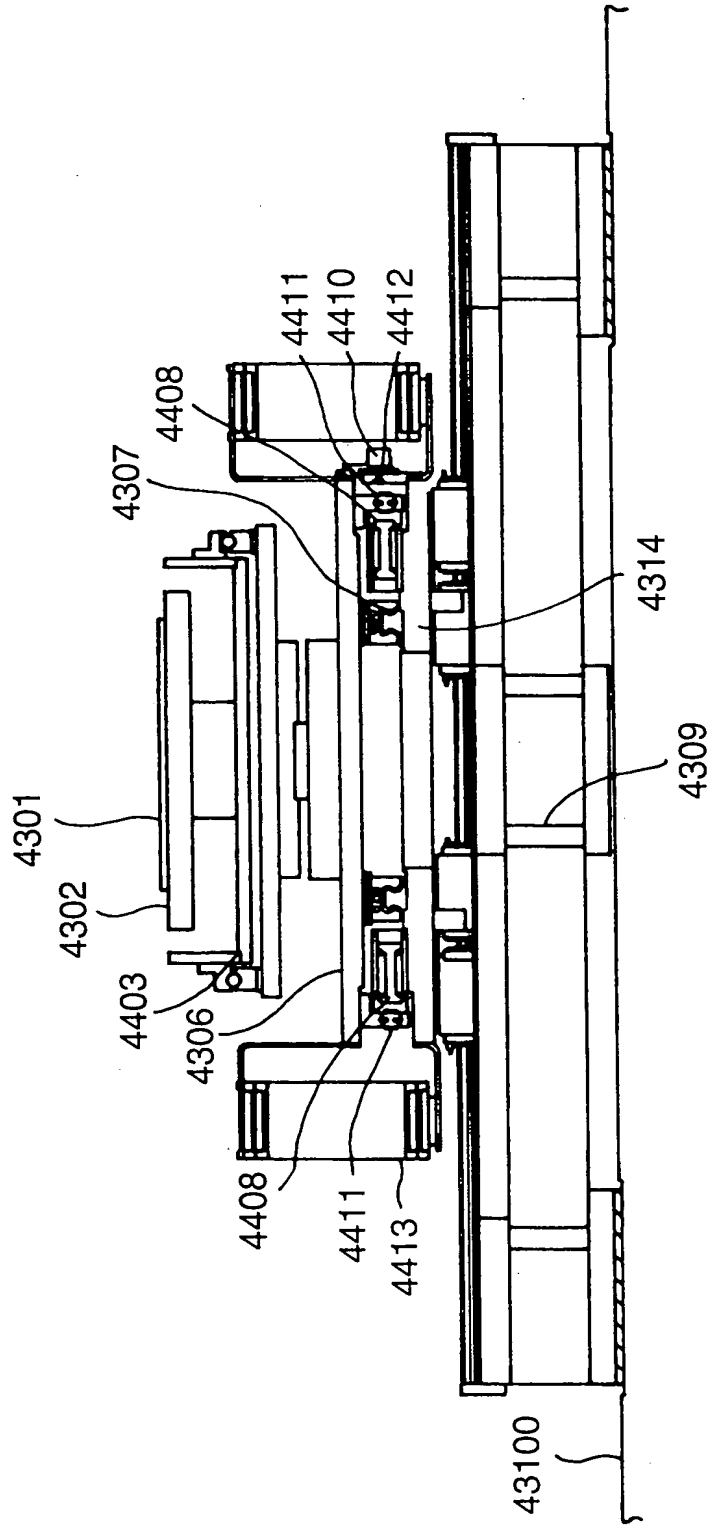


FIG.25





C-C

FIG.29

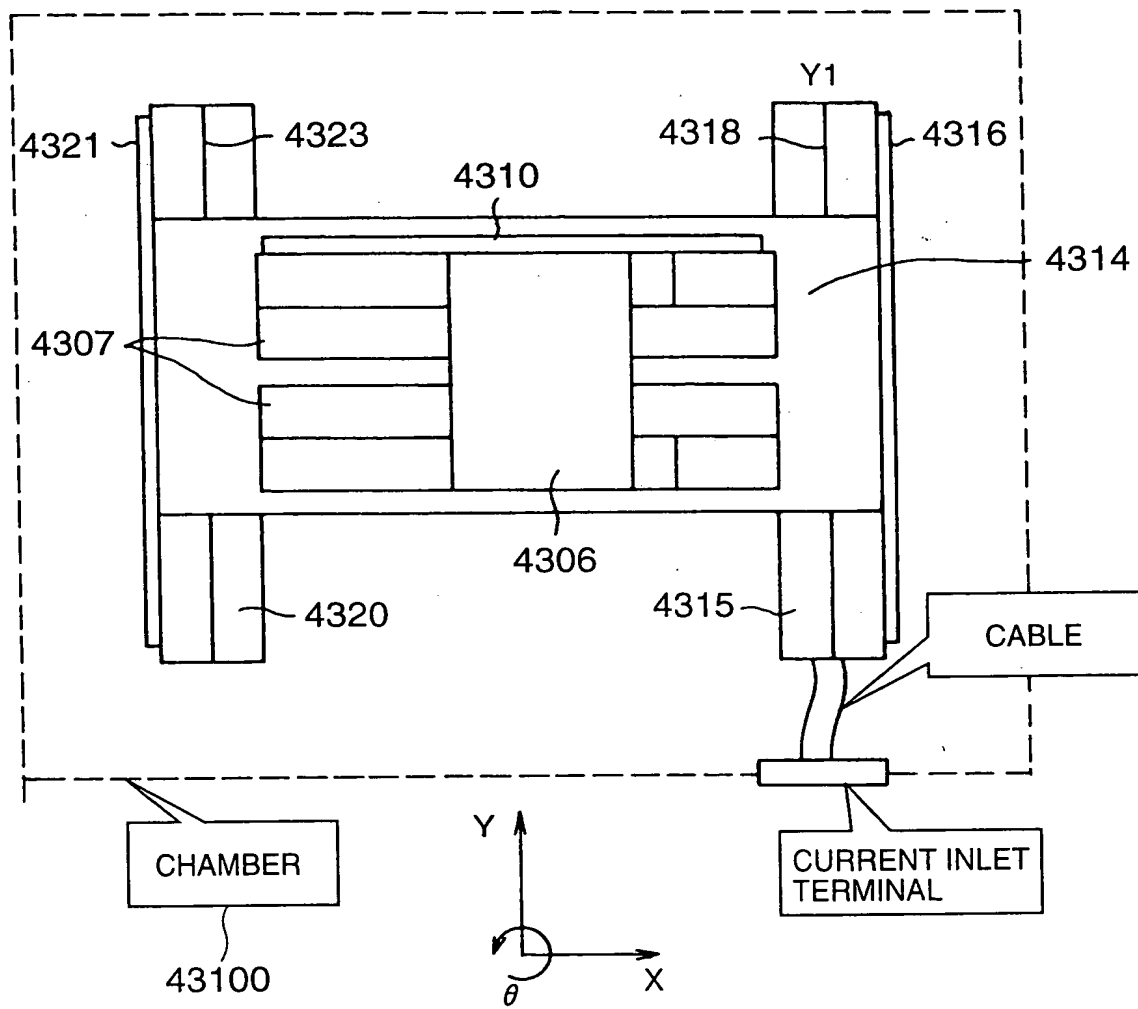


FIG.30

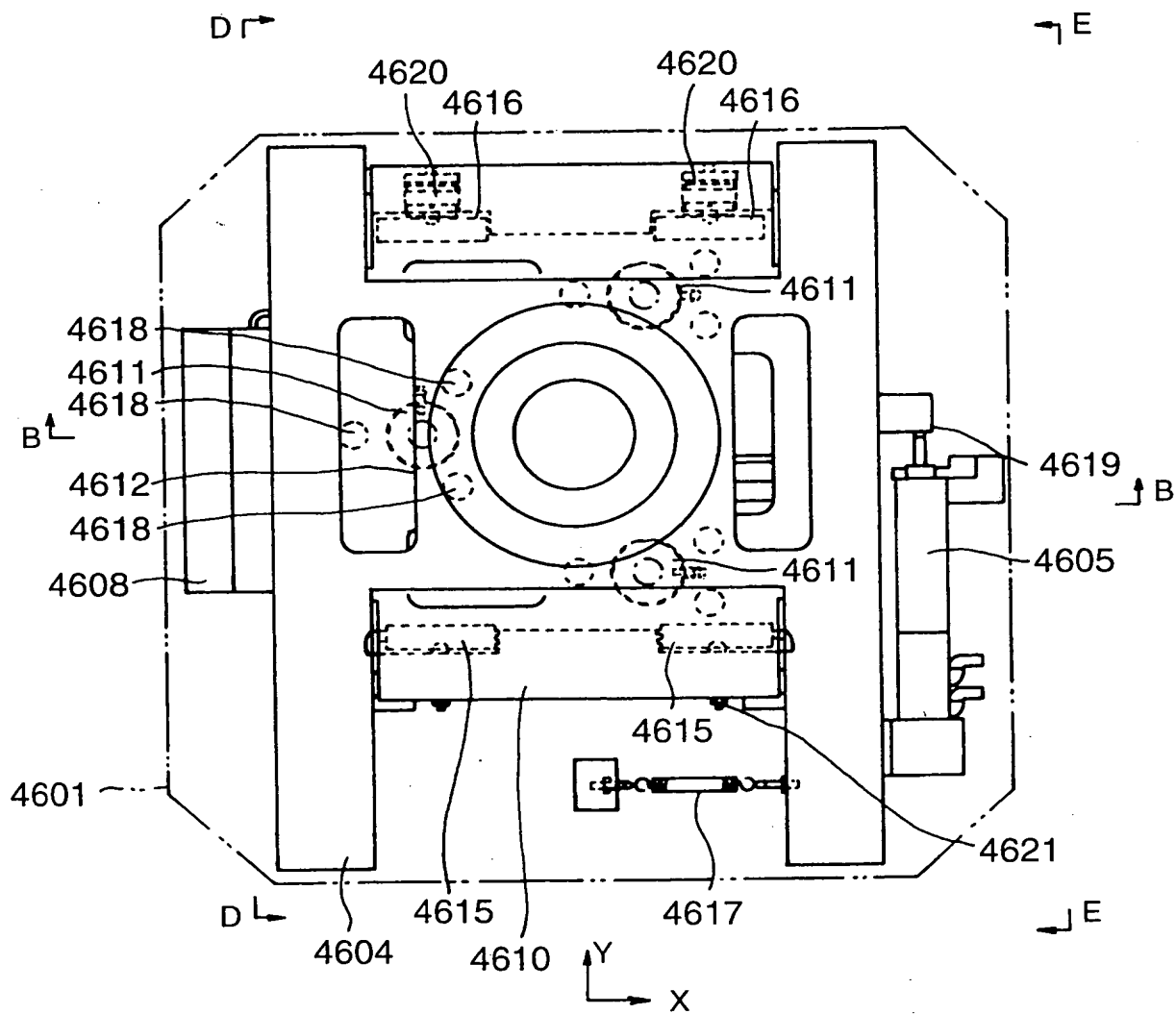


FIG.31

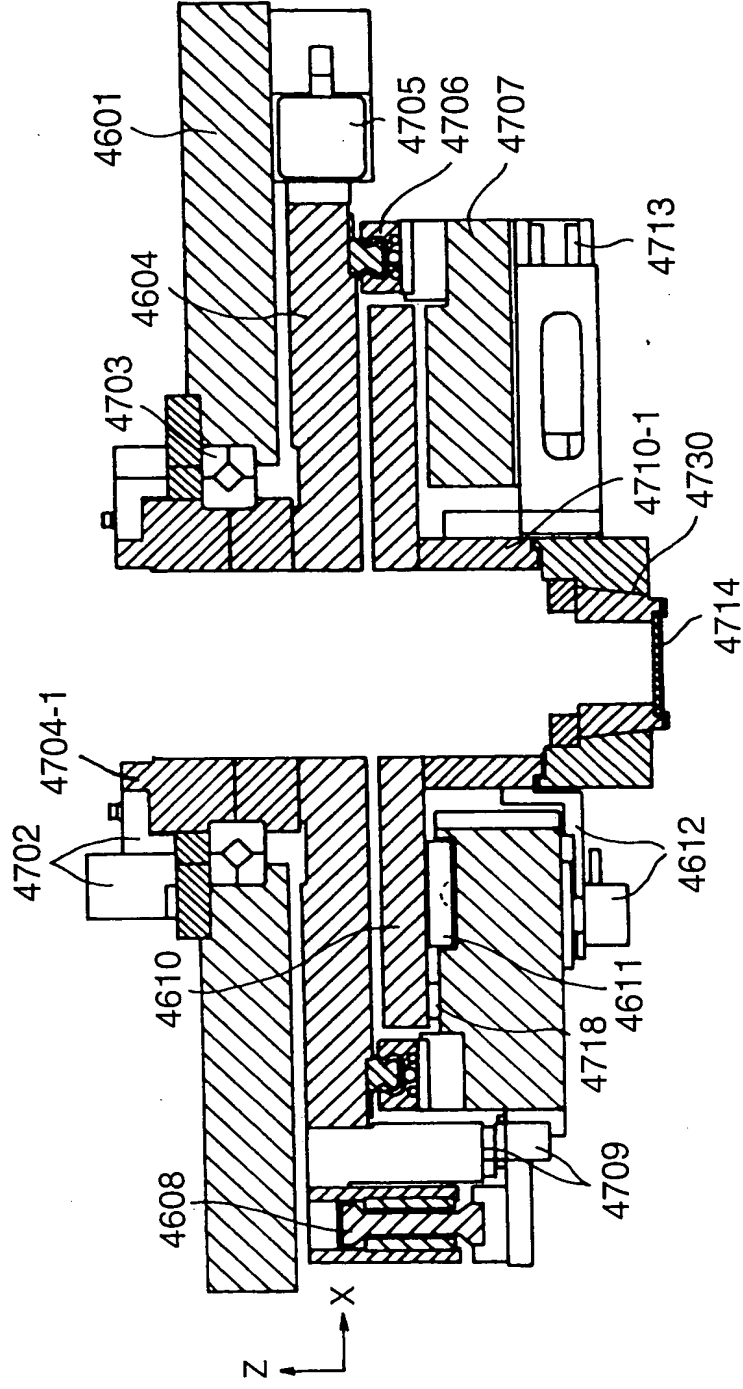


FIG.32

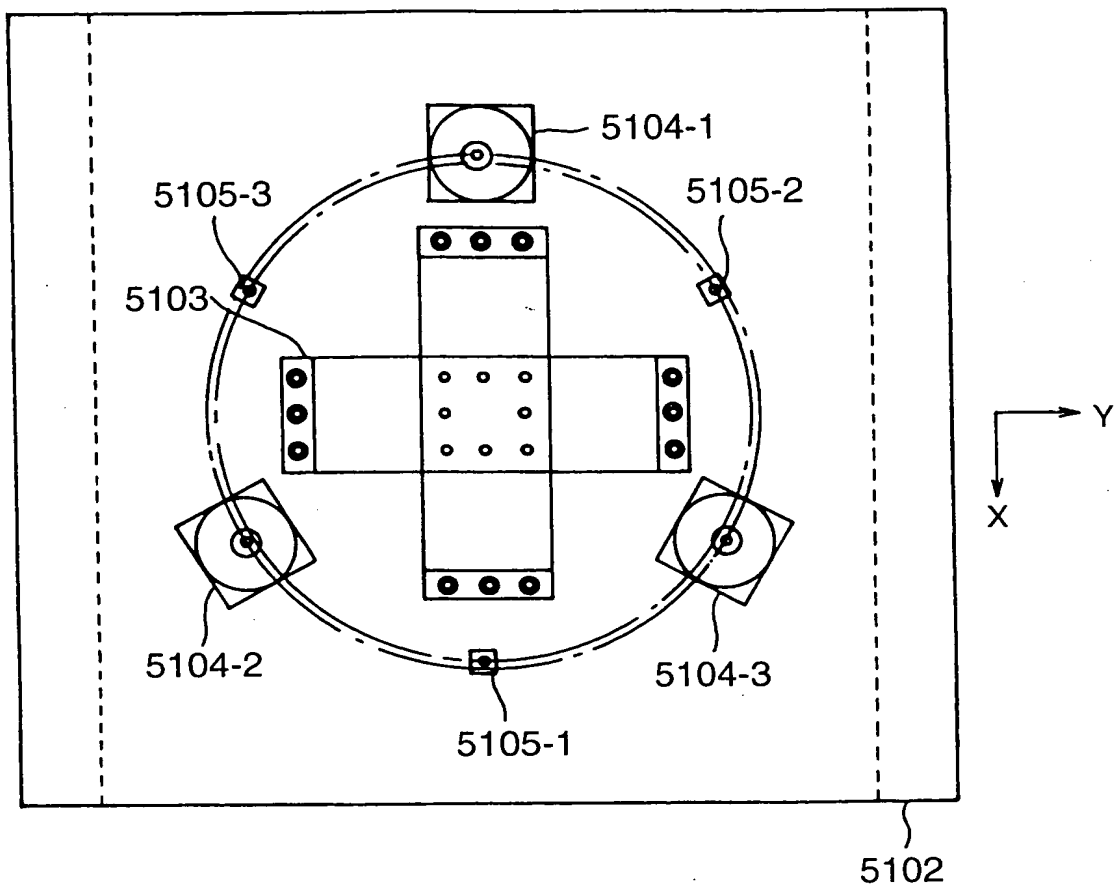


FIG. 33

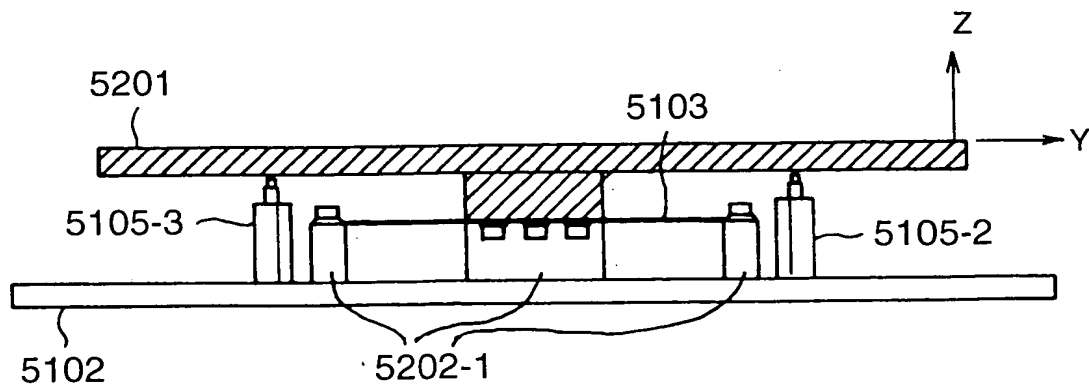


FIG. 34

FIG.35

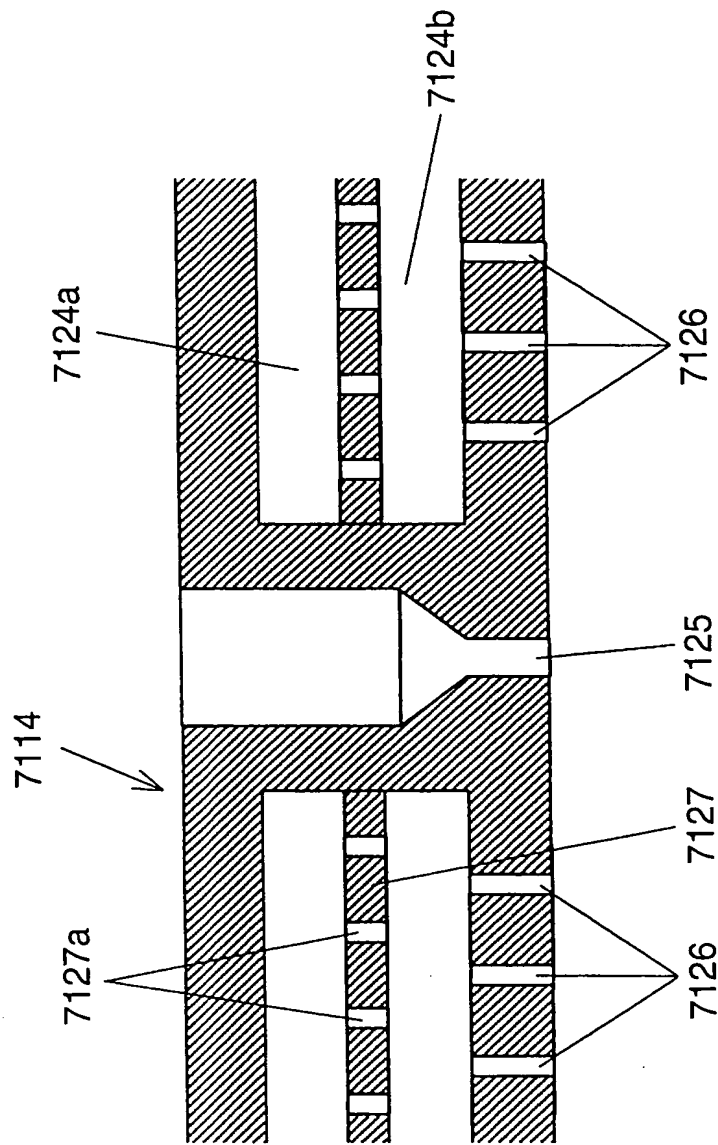


FIG.37

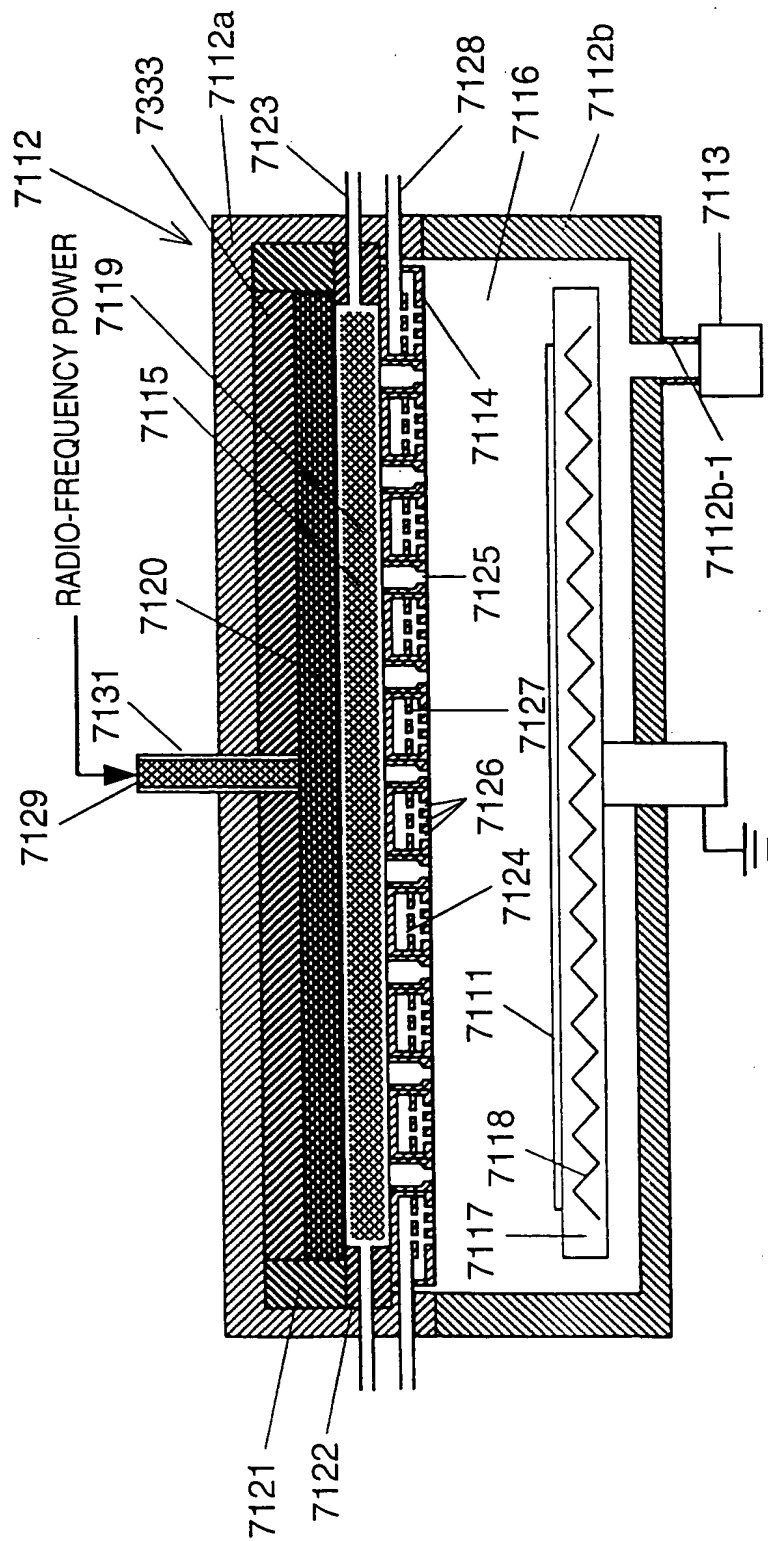


FIG.38

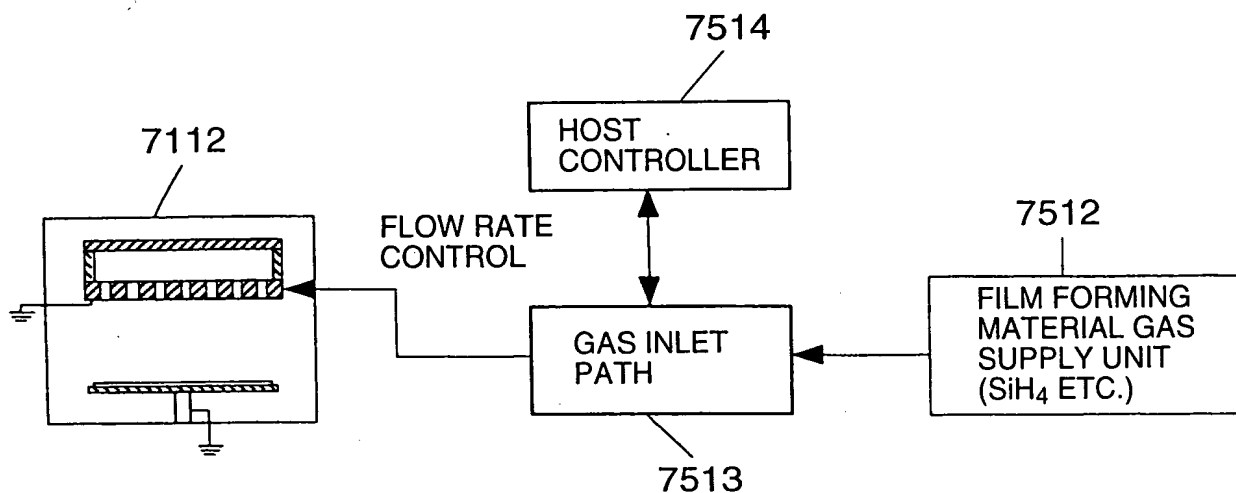


FIG.40

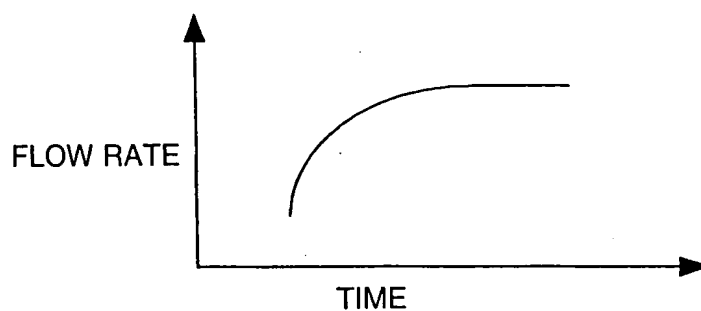


FIG.41

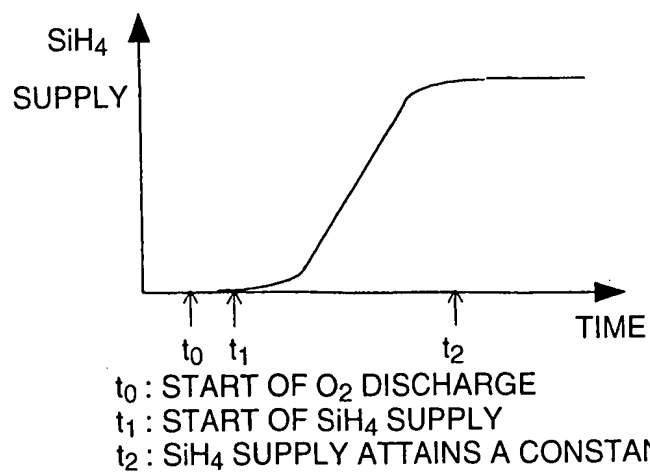


FIG.42

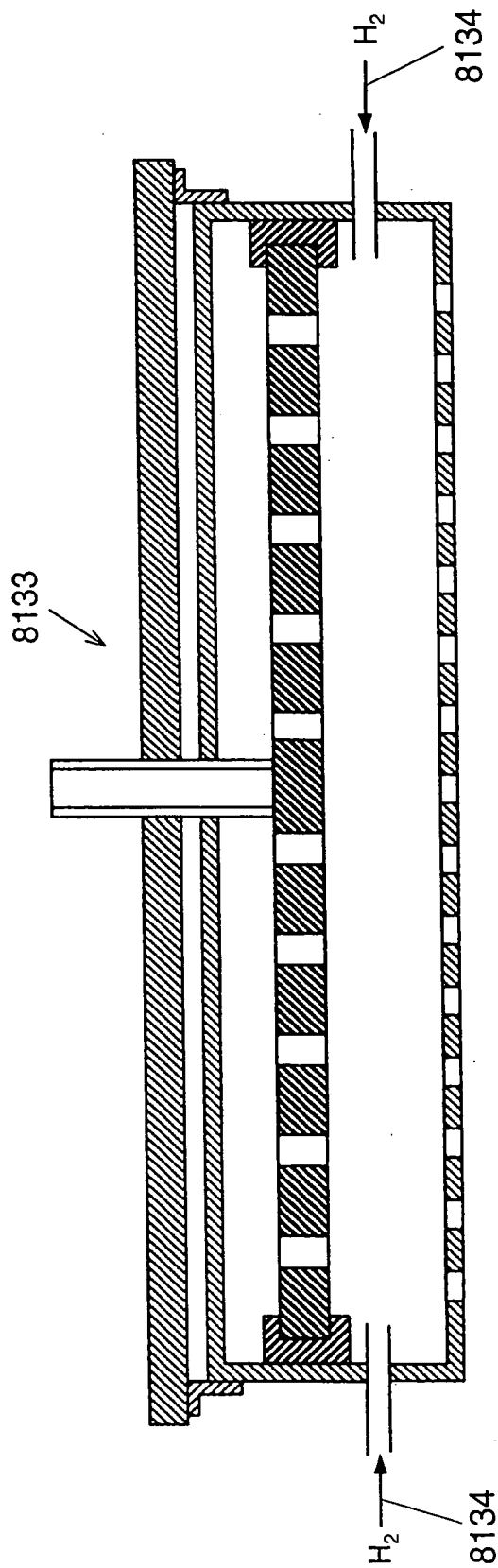


FIG:44

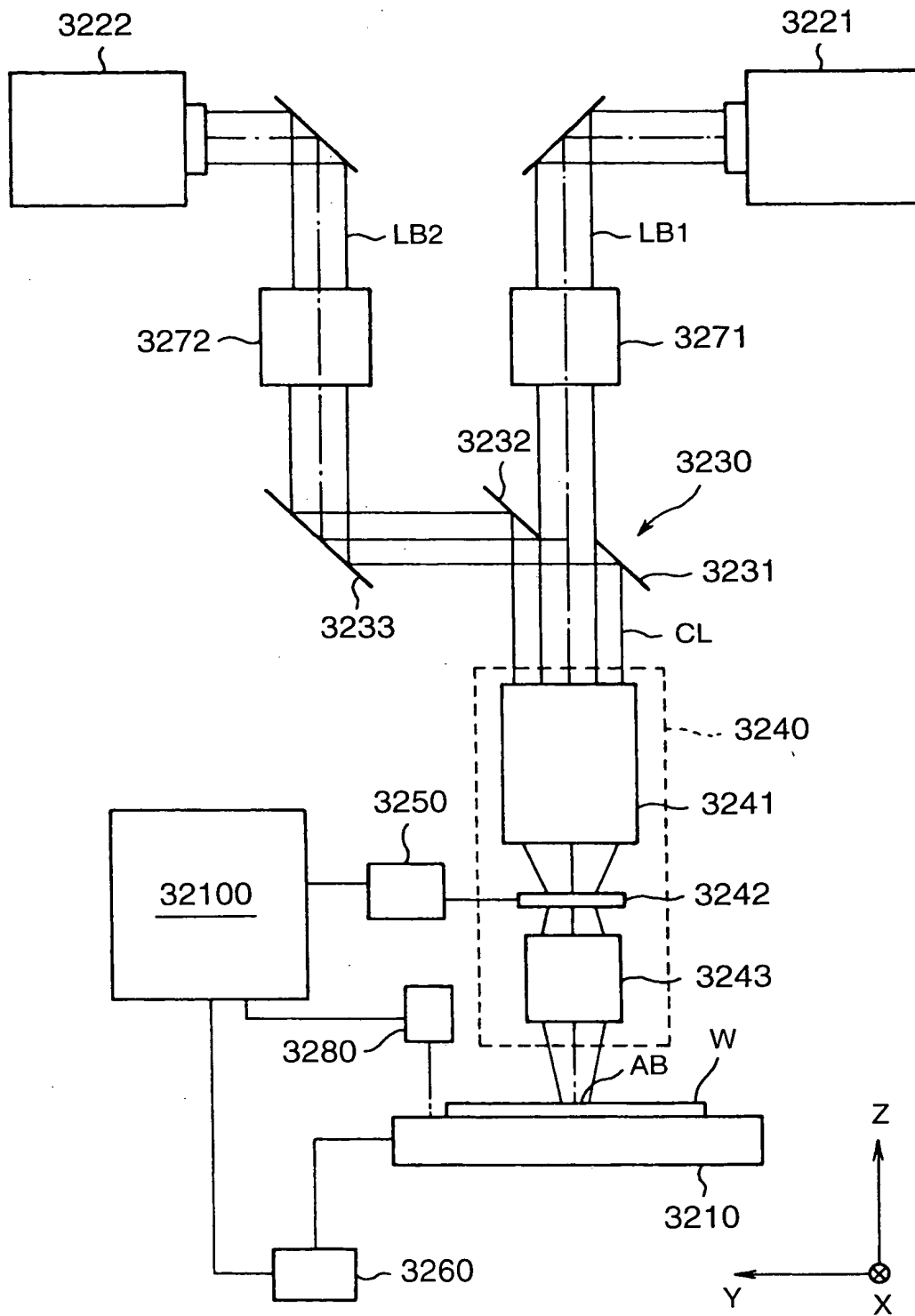


FIG.45

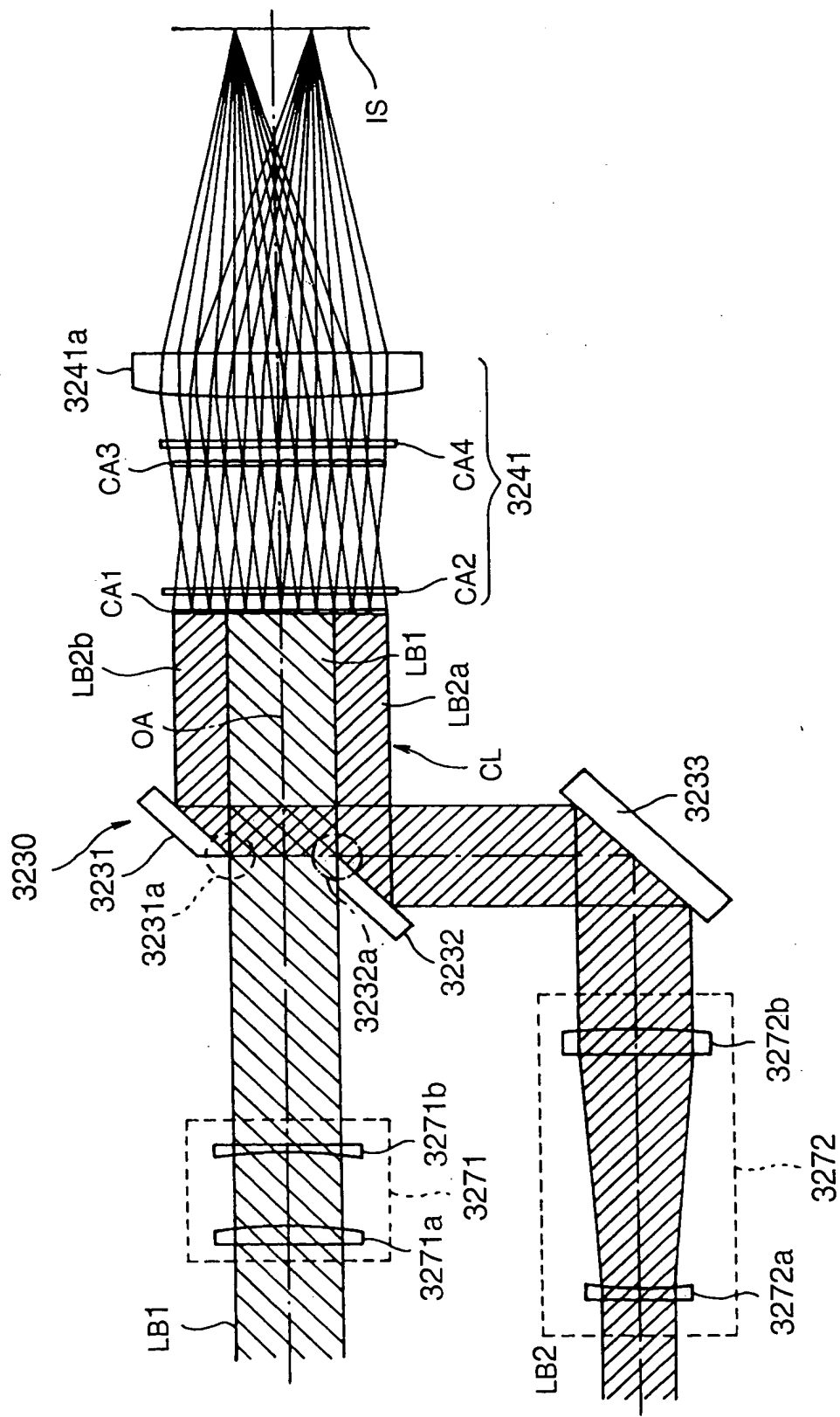


FIG. 46

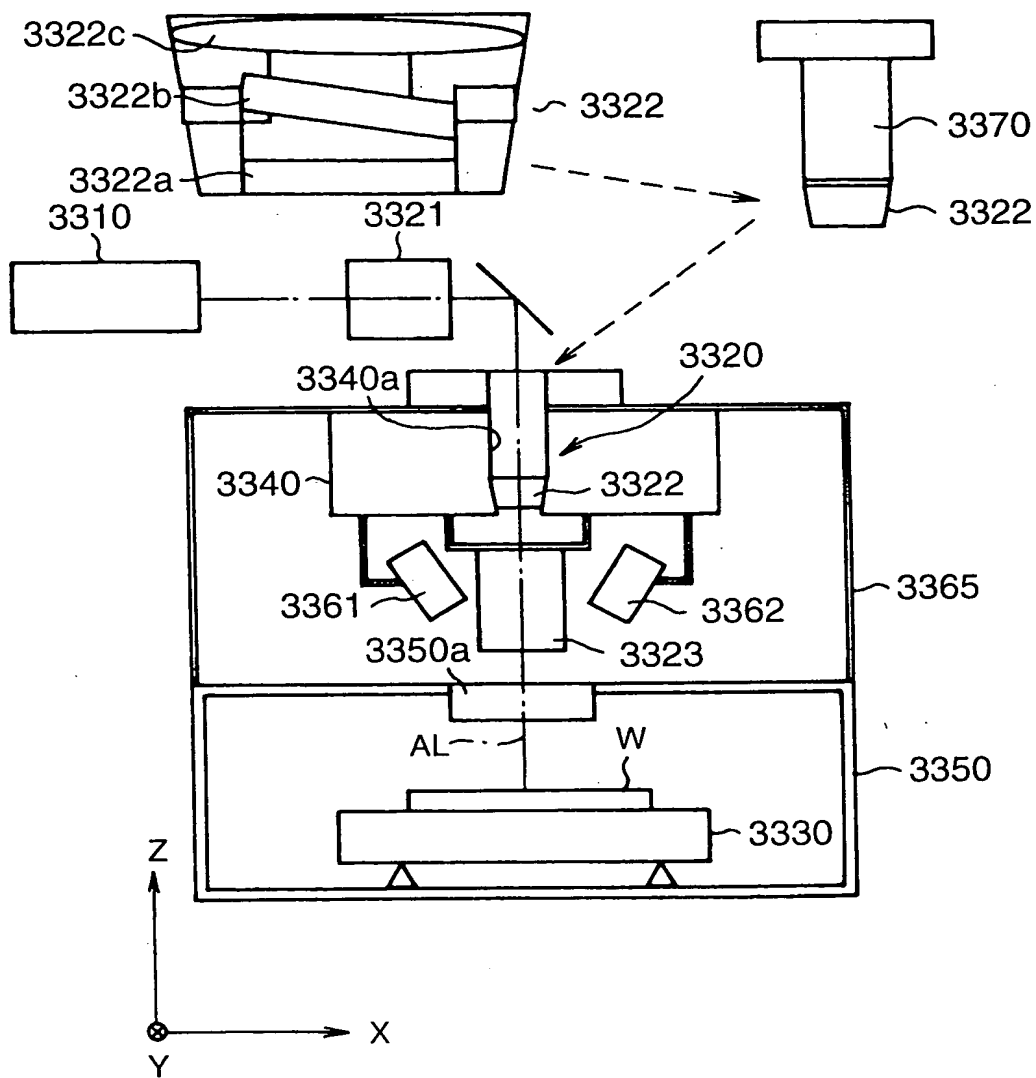


FIG.47

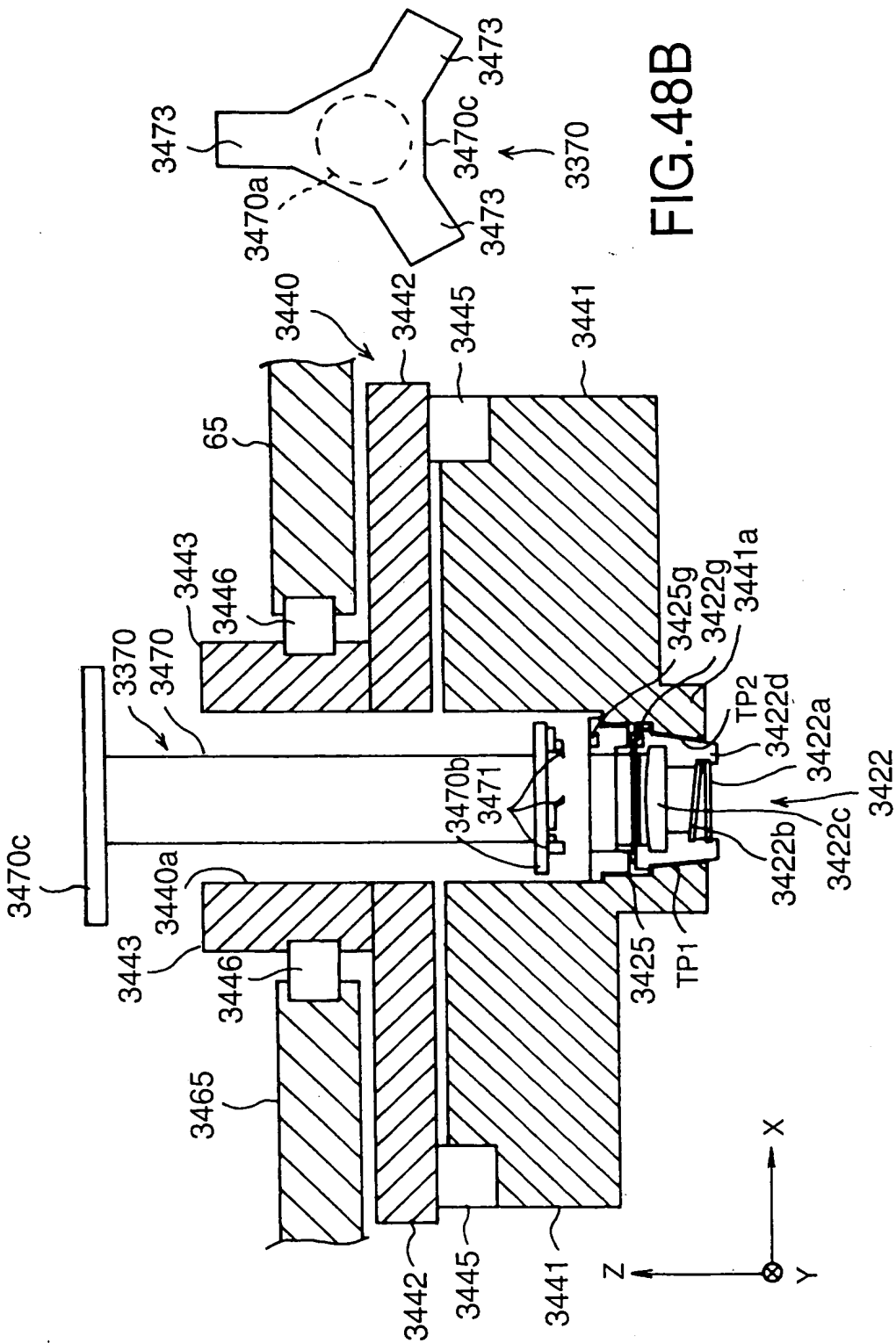


FIG. 48A

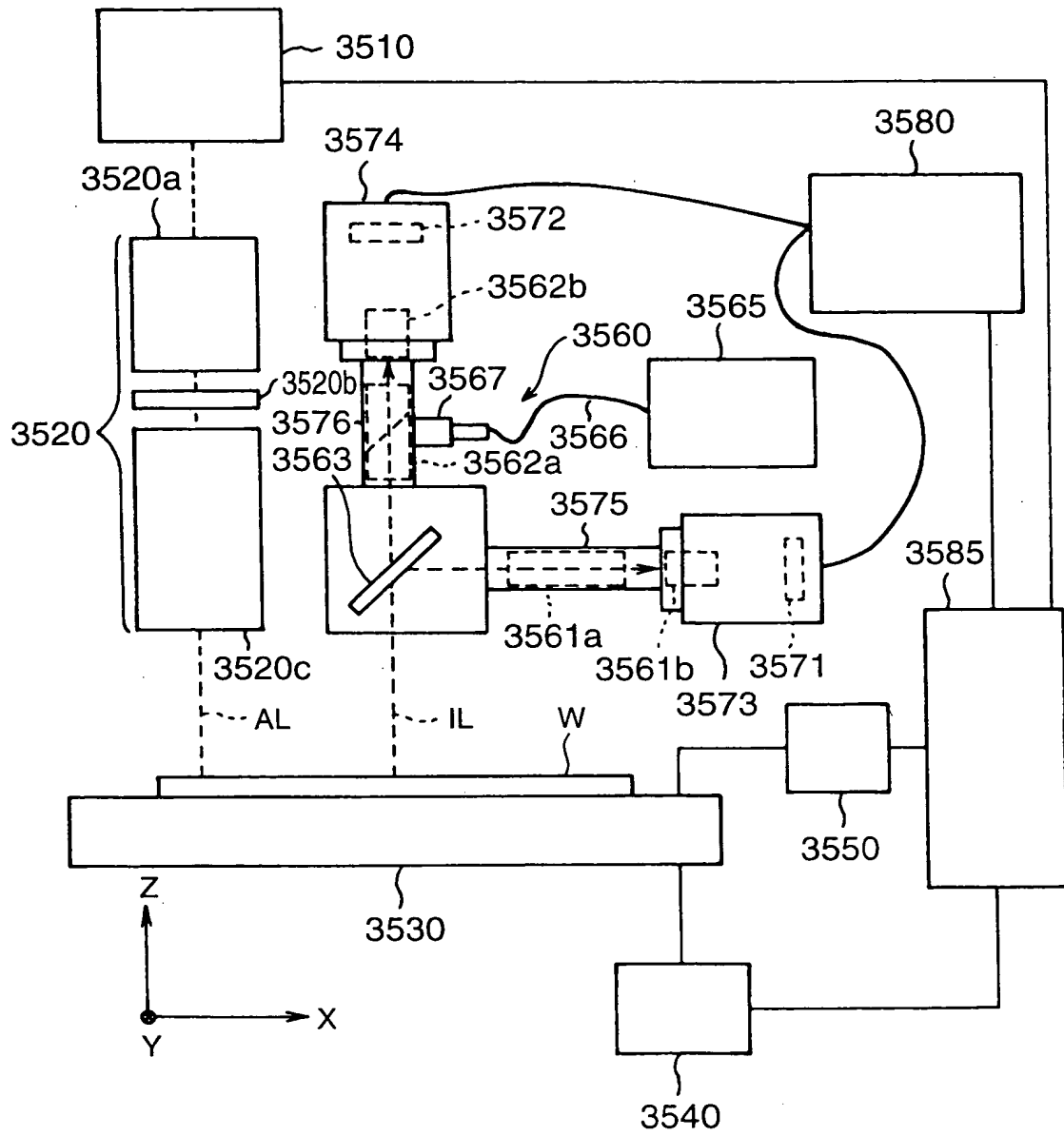


FIG.49

A schematic diagram of a rectangular device. The device is represented by a large rectangle. On the left side, there are two input ports, each represented by a cross symbol with a plus sign inside. The top input port is labeled 'M1' and the bottom input port is labeled 'M2'. On the top side, there is a label 'W' with a vertical line pointing to the top edge, indicating the width of the device.

[illegible]

FIG. 51



FIG. 52